High Speed Serial Trace Port Architecture Specification

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Abstract

This document specifies a Serial Transmit Port (STP) as a replacement for existing parallel data output port suitable for transmitting high bandwidth data off-chip such as from ARM's Embedded Trace Macrocells. This will lower ASIC pin count, increase possible bandwidth and, in some cases, reduce the silicon area.

This document covers the architectural definition of the STP. Please consult the relevant design documents or data sheets for each device for implementation details such as configuration options, power and area.

Keywords

Serial Transmit Port, Gigabit, Differential, Aurora

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1 ABOUT THIS DOCUMENT

1.1 Change control

1.1.1 Current status and anticipated changes

This specification has been developed by ARM based on a specification generated by Agere Systems Inc. and with consultation other signatories of the HSSTP Specification Participation Agreement.

1.1.2 Change history

Revision	Date	Comments
0.0	July 2, 2004	First Draft
0.1	July 15, 2004	Updated control and status interface
0.2	July 28,2004	Updated CoreSight to STP interface and miscellaneous changes
0.3	August 12, 2004	Updated to include STP PHY and Link
0.4	August 18, 2004	Updated to include Aurora link layer implementation details
0.5	September 8th, 2004	Updated for generalization of spec, remove board-to-board connection
0.6	September 10th, 2004	Updated with cable insertion loss data and DCD v1/v3 interfacing
0.7	October 8th, 2004	Updated STP/DCD interoperability section, reformatted to ARM Specification template.
0.8	November 15th, 2004	Specify bytes per lane, specify error requirements
0.9	November 16th 2004	Minor formatting and referencing updates
0.10	November 29th 2004	Added new section on reset methodology to ETM/Link section
2.0	February 1st 2005	Released version of 0.10
2.1	March 30th, 2005	Added information about unused bits in 24-bit mode and extra bits for STP control
2.2	January 23rd, 2006	Added confidential license terms
3.0	December 20th, 2006	Removed implementation specific information, change connector specification to ERM8/ERF8, move ETM and CoreSight usage examples to Appendix.
3.1	February 28th, 2007	Electrical characteristics refined (table 1), SSC modulation supported, reference clock frequency may be 1/20th, 1/25th or 1/30th of data bit rate, CRC check is optional, minor textual clarifications.
4.0	February 28th, 2007	Increased to major version, no changes
5.0	September 26th, 2008	Moved control and status registers to Programmers Model section, added extra control registers and revised texts for existing registers. Link layer protocol text expanded with details on data ordering, NFC and UFC messages. Added latch grounding to connector requirements and appendix to cover in more detail data ordering differences between

		CoreSight TPIU and the Aurora Protocol Specification.
5.2	January 30th, 2009	Change history corrected, legal disclaimer revised and minor clarifications to the definition of LINK_xLANE bits within LINK and PHY Capability register and the scope of the Error Detection calculation. Updated latching connector pictures and references to Aurora Protocol Specification v2.0.

1.2 Confidentiality status

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1.3 References

This document refers to the following documents:

Ref	Date	Author(s)	Title
1	May 5th 2004	Fibre Channel Industry Association	Fiber Channel Physical Interfaces, FC-PI, Rev. 5.0,
2	March 22nd, 2004	Serial ATA International Organization	Serial ATA Electrical Specification, Rev 1.0,
3	September 19th, 2007	Xilinx Corporation	Aurora Protocol Specification SP002 (v2.0)

1.4 Terms and abbreviations

This document uses the following terms and abbreviations:

Term	Meaning
CoreSight	The infrastructure for monitoring, tracing, and debugging a complete SoC.
CRC	Cyclical Redundancy Check
DCD	Data Collection Device, for capturing data transmitted out of the STP.
ETM	Embedded Trace Macrocell, generating real-time instruction and data trace of an ARM processor.
Gbps	Gigabits per second
IMPLEMENTATION DEFINED	The behavior is not architecturally defined, but it is defined and documented by individual implementations.
Lane	One differential signal pair and the associated serial transmitter
LINK	Data Link Interface Layer
LSB	Least Significant Bit
MSB	Most Significant Bit
NRZ	Non-Return to Zero
PCB	Printed Circuit Board

PHY	Physical interface layer
PLL	Phase Locked Loop
RAZ/SBZP	Reserved as Zero / Should Be Zero or Preserved
Rx	Receiver
SAS	Serial Attached SCSI
SATA	Serial Attached Trade Association
SoC	System-on-Chip, MCU, ASIC or FPGA, containing the STP
STP	Serial Transmit Port
DCD	Data Collection Device. A device for capturing the data transmitted out of the STP.
SSC	Spread Spectrum Clocking, modulation used in PCI Express and SATA
TPA	Trace Port Analyzer, a legacy device for capturing data from parallel trace ports.
TPIU	Trace Port Interface Unit. The TPIU acts as a bridge between the on-chip trace data source and the data stream transmitted by the STP.
Tx	Transmitter
UFC	User Flow Control

2 SCOPE

This document specifies a Serial Transmit Port (STP) as a replacement for existing parallel data output port suitable for transmitting high bandwidth data off-chip such as from ARM's Embedded Trace Macrocells. This will lower ASIC pin count, increase possible bandwidth and, in some cases, reduce the silicon area.

This document covers the architectural definition of the STP. Please consult the relevant design documents or data sheets for each device for implementation details such as configuration options, power and area.

Appendices A, B and C are informative only.

A block diagram is shown in Figure 1:

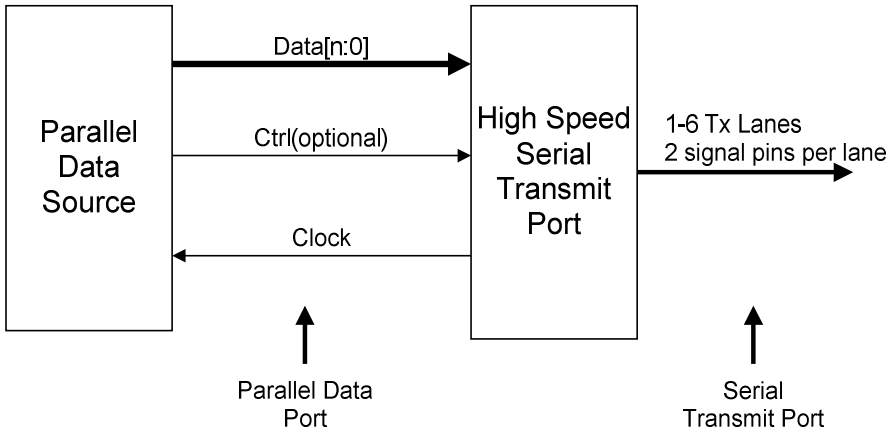


Figure 1: STP overview

Note For example, a 16-bit parallel trace port requires 17 or 18 signal pins plus power and ground pins. The serial port requires 4 signal pins plus power and ground pins for two lanes of data giving equivalent bandwidth. Since clock is encoded with the data, the clock/data skew problems inherent in the parallel port are not present in the serial port.

3 INTRODUCTION

Transferring data off chip for high performance embedded microprocessor cores requires a data port with sufficient data bandwidth. Traditional parallel port implementations typically employ a clock synchronous parallel interface, using as many as 32 parallel data lines at clock speeds up to 300 MHz to provide the required bandwidth. Increasing CPU clock speeds and use of multiple processor cores demand increasing data port bandwidth, while at the same time the number of I/O pins used for the data port should be reduced to facilitate lower cost and a higher level of SOC/ASIC integration.

A serial implementation of the data port (Serial Transmit Port, STP), taking advantage of available high-speed serial interface technology used in SATA, PCI Express, XAUI and Fibre Channel, can provide higher transmit bandwidth with fewer I/O pins compared to a parallel implementation.

The STP consists of two layers: PHY and LINK as shown in **Error! Reference source not found.**. The number of lanes may vary between 1 and 6.

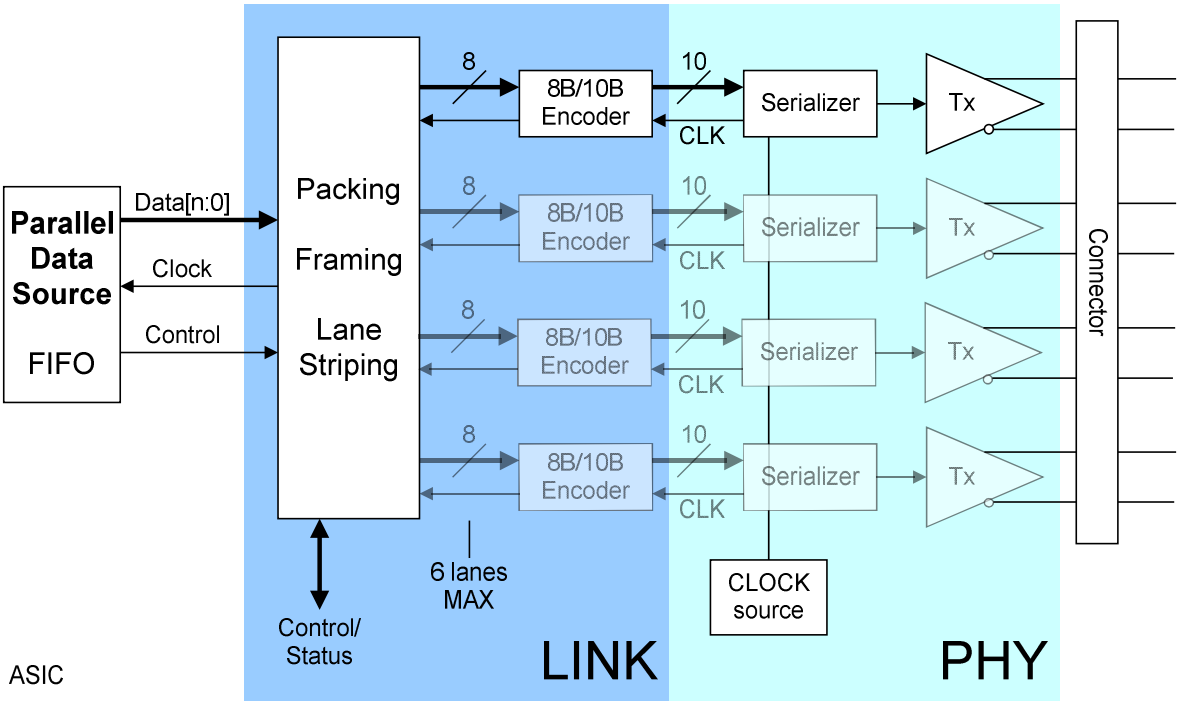


Figure 2: STP Block Diagram

4 PHY LAYER

This section describes the characteristics of the PHY aspect of HSSTP. It includes tolerances of the PHY transmitter, the supported clock configurations and interoperability.

For any programmers model information see section 6.

4.1 Electrical Interface Characteristics

Table 1 details the allowable electrical and clock characteristics for a PHY conforming to the HSSTP Architecture.

Table 1: Overview of STP PHY electrical interface characteristics

Parameter	**STP PHY**
Supported Bit Rates	2.5, 3.0, 3.125, 4.25, 5.0, 6.0 and 6.25 Gbps*
Clock tolerance	100 ppm
Topologies Supported	Point-to-point (multiple lanes)
Number of lanes	1 to 6 lanes
Line Code	NRZ
Data Encoding	8B/10B
Physical link bit error rate	≤ 10E-13
Duplex	No duplex, unidirectional channels from SoC to DCD
Signaling	
Characteristic Impedance (Termination)	100 ohm differential
Coupling	AC coupled on Rx side
Transmit Signal Level (transition bit amplitude)	1600 mV_{p-p} max. 400 mV_{p-p} min.
Transmit De-Emphasis	0%-30% (below transition bit)
Jitter Generation (Total)	0.4UI
Jitter Generation (Deterministic)	0.2UI
Receive Clock Level (Differential p-p) (option C)	1600 mV_{p-p} max. 200 mV_{p-p} min.
Receive Clock Duty cycle (option C)	47.5%-52.5%

* Frequencies selected are those commonly used in SerDes designs for SAS/SATA, XAUI, PCI Express and Fibre Channel. The frequency of operation of the STP is likely to be governed by the frequency of other SerDes implementation deployed in the SoC/ASIC. The frequency of operation of the Data Collection Device (DCD) must match that supported by the STP. The technology presently available to DCD designers requires that a crystal clock at the DCD match that of the STP. Due to this and other implementation issues, some DCD implementations may only support a subset of the permissible bit rates. The DCD should support Spread Spectrum Clocking (SSC) modulation with a nominal frequency shift from +0% to -0.5% of the clock frequency.

4.2 Functional Description

The STP PHY performs the following primary functions:

- Serialize 10-bit parallel input symbols from the 8B/10B encoder (not part of the STP PHY)
- Transmit a differential NRZ serial stream at specified data rate and with the specified transmit signal characteristics through the differential transmit driver(s) (one to six transmit lanes)
- Provide a 100 Ohm (nominal) differential termination impedance at the transmitter driver outputs
- Perform proper power-on sequencing
- Provide device status information to link control logic
- Provide clocks to the 8B/10B encoder and other circuits as required

Secondary functions depend on the configuration:

- In configurations A and B (see section 4.4.1 and section 4.4.2 respectively)
    - Synthesize the required high-speed transmit bit clock from a lower frequency reference clock signal
- In configuration C (see section 4.4.3)
    - Provide a low-voltage differential receiver with 100 ohm differential termination impedance
    - Use the half-rate clock signal received at the receiver as the high-speed transmit bit clock for the transmitter.

4.3 Lane Configuration

The STP PHY design may implement between 1 and 6 transmit lanes with a single set of common PHY blocks such as bias circuitry and transmit clock PLL (in configurations A and B) or bit clock receiver (in configuration C).

When more than one lane is implemented, the serializers of all lanes shall be synchronized to a single common 10B symbol clock.

In order to unambiguously specify which configuration is required for an SOC, the various possibilities shall be identified as:

STP_PHY_[Configuration Letter][Number of Lanes]

For example: STP_PHY_A1, STP_PHY_C3

4.4 PLL and Clock Configurations

Three clock configurations are described below. The STP PHY implementation shall support one of the three allowable configurations and indicate which configuration through the setting of status bits in the LINK and PHY Capability Register, see section 6.7.

Configurations A and B are intended for use when another SerDes PHY is present in the SoC and common PHY blocks such as bias circuitry and transmit clock PLL can be re-utilized.

Configuration C is intended for design containing no other high speed PHY and where the signal integrity requirements necessary to achieve the bit error rate objective can be safely met without negating the area saving due to the omission of the transmit clock PLL. Note that the additional pins required for the differential receiver are offset by the PLL power and ground pins which are no longer required.

4.4.1 Configuration A

A transmit clock PLL in the SoC generates the high-speed serial bit clock from an internally supplied reference clock signal for use by the STP PHY macrocell, as shown in Figure 2 .

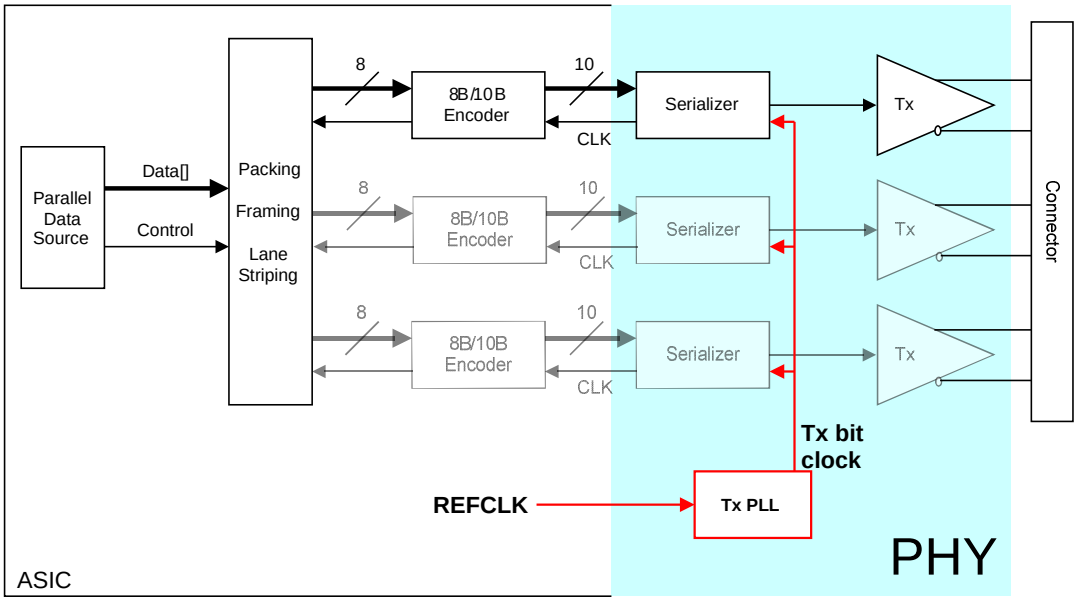


Figure 2: Example configuration A – internal reference clock

4.4.2 Configuration B

A transmit clock PLL in the SoC generates the high-speed serial bit clock from an externally supplied reference clock signal for use by the STP PHY macrocell as shown in Figure 3. This reference clock may be supplied either by the DCD or from any other source. Provision has been made in the connector for this signal.

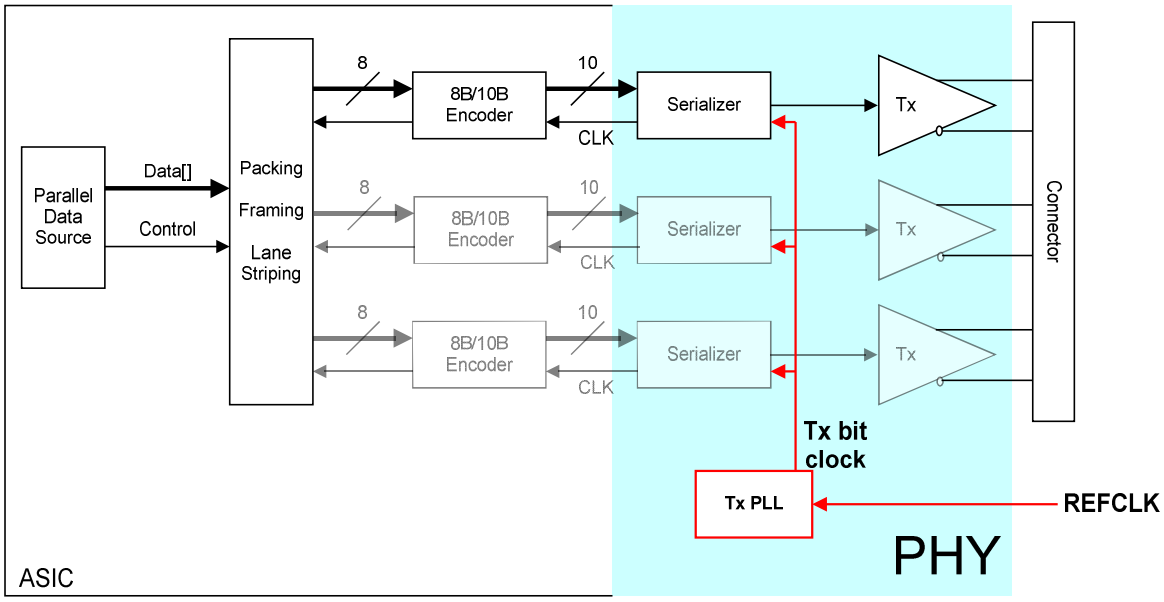


Figure 3: Example configuration B – external reference clock

4.4.3 Configuration C

High-speed serial bit-clock supplied externally through a low voltage, differential signal receiver as shown in Figure 4.

The frequency of the external bit clock shall be half the transmit data rate, for example, for 3 Gbps transmit data rate the bit clock frequency shall be 1.5 GHz.

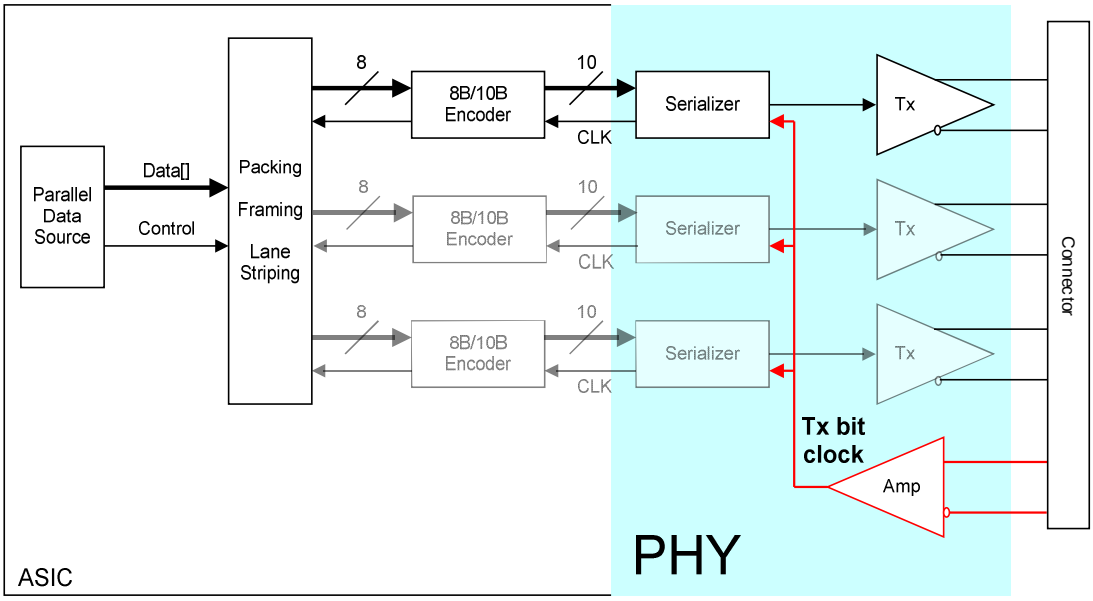


Figure 4: Example configuration C - external high-speed bit clock

4.5 Clock Constraints

The STP PHY interfaces to a Data Collection Device, DCD. The available technology (as of 2006) requires that the Tx clock shall match the Rx clock to within 100 ppm.

4.5.1 Configuration A

The Tx clock shall match the Rx clocks to within 100 ppm.

4.5.2 Configuration B

The reference clock may be supplied by either the DCD or from another source. This configuration may be used when a suitable clock and PLL combination is not available on the ASIC.

4.5.2.1 Reference clock from the DCD

The DCD shall provide a differential reference clock frequency of 1/20th or 1/25th or 1/30th of the Tx bit rate. The choice of frequency is made by the configuration of the DCD. The duty cycle and jitter requirements shall be as shown in Table 2.

Table 2: Reference clock duty cycle and jitter requirements

Parameter	Symbol	Min	Typ	Max	Units
Duty Cycle	DC_j	47.5	—	52.5	%
Cycle to cycle Jitter	$T_{CCJITTER}$	—	—	150	ps p-p
Total Jitter 1KHz – 1MHz	$J_{TOTALlow}$	—	—	100	ps p-p
Total Jitter 1MHz – 20MHz	$J_{TOTALmid}$	—	—	40	ps p-p
Total Jitter > 20MHz	$J_{TOTALhigh}$	—	—	100	ps p-p

4.5.2.2 Reference clock not from the DCD

The Tx clock shall match the Rx clocks to within 100 ppm.

4.5.3 Configuration C

The DCD provides a differential clock of half the Tx bit rate. The total jitter allowed on this clock is 0.2UI with up to 0.1UI allowable deterministic jitter.

The electrical characteristics of the high-speed differential bit clock receiver are specified in Table 1.

4.6 Interoperability Requirements

The STP PHY transmit signal characteristics shall support cabled (see “Cables and Connectors”, below) interconnects to a receiver, and in the case of configuration C, a transmitter of the high-speed bit-clock signal.

- Through two connector pairs and a cable designed or empirically determined to be suitable to support the relevant data rates
- A maximum cable length of 15 cm should be assumed, though longer cables may be supported e.g. for in-rack target systems

4.7 Hot Plug-ability

The STP PHY macrocell shall also be designed for hot plug-ability and any design aspects considerations to realize this feature should be kept in mind while designing the macrocell.

5 LINK LAYER

The STP link layer consists of all the necessary circuitry to convert the parallel data source into 10B symbols suitable for input to the PHY layer serializer. The link layer distributes the data among the number of lanes implemented in the design (between 1 and 6) and provides a link format sufficient to re-join the lanes (channel bonding) at the receive side in the Data Collection Device (DCD). The order of the trace packets shall not change although the timing of arrival may change.

Note No timing information can be inferred from the timing of the arrival of data packets at the DCD.

This section does not describe any programmable registers; refer to section 6 for the programmer's model to the STP.

The link format is specified in section 5.1, error conditions that can be detected by the DCD are defined in section 5.3 and reset requirements are defined in section 5.4.

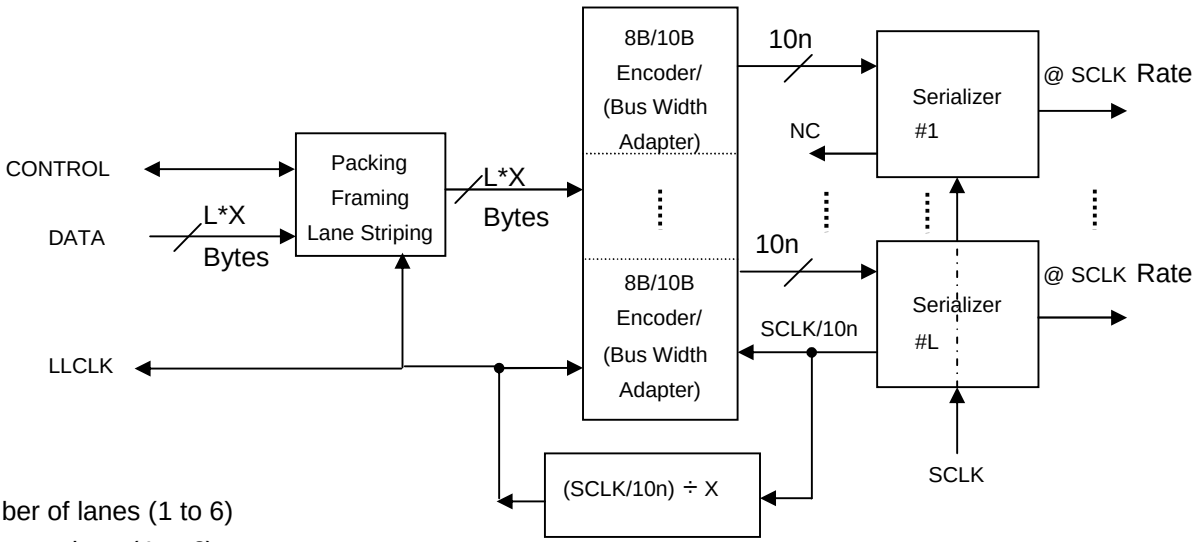
An example implementation showing how parallel data from an ARM ETM or CoreSight system should be represented within the link layer is given in Appendix B.

5.1 LINK Specification

The STP link layer shall implement the serial simplex operation, 8B10B encoding of the Xilinx Aurora Protocol Specification v1.3. Please consult the Aurora protocol specification [3] for details.

This section contains information about the application of the Aurora protocol to the STP and augments information in the Aurora protocol specification.

5.1.1 STP Tx block diagram



L = number of lanes (1 to 6)

X = bytes per lane (4 or 2)

n = number of 8B/10B encoders per serializer

Figure 5: Link layer Tx block diagram

Note The DCD Rx block should always be able to support 4 bytes per lane and may have a different value of n to the STP

5.1.2 Data frame format

The data frame format is a function of two variables:

1. L*X, the number of lanes multiplied by the number of bytes per lane.
2. Whether UFCs (see below) are present or not.

Figure 6 is an example frame which includes trace message bytes (A and B), a UFC message and optional padding byte which is only present when the sum of data sections A B is an odd number of octets. The total number of octets of user data (A+B) per Aurora frame is IMPLEMENTATION DEFINED.

Start of Frame (2 octets)	User Data (A octets)	UFC Header (2 octets)	UFC message (2 octets)	User Data (B octets)	CRC (2 octets)	Padding (1 octets - optional)	End of Frame (2 octets)

Figure 6: An Aurora frame with a Trigger UFC message

Note Presence of the two octets for the CRC value is indicated within LINK_NOCRC, see LINK and PHY Capability Register in section 6.7.

5.1.2.1 Error detection

A cyclic redundancy check (CRC) should only be used on the entire frame content of user data to ensure correct data in the frames. Any UFC packets (including payload message), idle packets, clock compensation sequences or padding octet should not be included in the calculation. The polynomial used shall be:

Polynomial: $G(x) = X^{16} + X^{15} + X^2 + 1$

Initial value: 0xFFFF

5.1.3 NFCs and UFCs

NFC & UFC are Native Flow Control and User Flow Control; they can be used within the Aurora link layer to manage the data being transmitted. The STP does not use messages for flow control management. A limited set of UFC messages are allowed within the HSSTP Architecture to indicate trace related information that a receiving TPA can utilize.

Only the following information types are defined:

- Trigger
- FIFO overflow
- Auxiliary information

The generic UFC format is shown in Figure 9. These UFC events should be considered rare and so will not consume significant bandwidth.

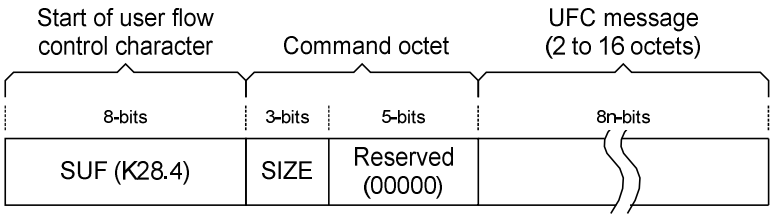


Figure 8: Generic UFC format

Triggers occur once per data capture and FIFO overflow is a catastrophic error condition which should not occur. The meaning and use of the Auxiliary UFC is IMPLEMENTATION DEFINED.

5.1.3.1 Trigger UFC

A Trigger UFC can be sent to indicate where within the trace data stream a trigger condition occurred. The location of the byte is conveyed in terms of the number of link layer octets of user data from the start of the current Aurora frame.

The Trigger UFC message uses SIZE = 3'b000 (2 octets) and the 2 message bytes convey the location of the trace data byte in the data frame that has trigger information associated with it.

It is acceptable for an implementation to never output this UFC message if there are other mechanisms able to convey this information, for example as part of the underlying trace data format.

5.1.3.2 FIFO overflow UFC

This message is used to indicate a transmit FIFO has overflowed. Since FIFO overflow is a catastrophic condition which should not occur, the complete STP/DCD system must be reset to continue normal operation.

The Overflow UFC message will indicate SIZE = 3'b111 (16 octets) and shall have 16 bytes of data where each byte in the message shall be 8'b00001010 (0x0A).

For more on the Aurora Simplex UFC interface, refer to the Data Control block description in the Aurora Protocol Specification v2.0 [3]. Where the STP is has the capability of performing flow control on the incoming trace data stream, it is recommended that implementations should not output the FIFO overflow UFC and should instead stall the trace data until the STP can continue accepting data. Under these circumstances, an STP implementation does not have to support the transmission of this UFC message.

5.1.3.3 Auxiliary UFC

This is a UFC message where the interpretation of the data contents is IMPLEMENTATION DEFINED. Tools should not require decoding of this in order to interpret the data being transmitted. It should only be used to transmit secondary information that does not affect the understanding of the trace data.

The Auxiliary UFC shall use the SIZE = 3'b001 (4 octets) and transmit 4 bytes of data where the message data is IMPLEMENTATION DEFINED.

For example, the UFC message could be used to indicate that the internal power demands of the system has changed with the data indicating the new power level and a domain reference to indicate which area of the ASIC.

5.1.3.4 Other UFC encodings

Other UFC encodings are reserved.

5.1.4 Clock Compensation

The Aurora Protocol Specification v2.0 [3] defines that the clock compensation sequences should be output at least once every 10,000 code groups. Implementations can choose to output clock compensation more regularly than this and even allow for it to be controlled through a programmable register.

Outputting the sequence more often than necessary will allow for accurate alignment with the transmit clock at the receiver end but at the reduction of allowable trace data bandwidth.

Note If an implementation outputs the clock compensation sequence more than 10,000 code groups separation, the receiver is at risk of losing synchronization with the STP. This can result in corrupted or lost trace data.

5.2 Trace data ordering

The only constraint imposed by the Aurora Protocol Specification v2.0 [3] on data ordering is that each octet is transmitted MSB first.

For example, the Start of Channel PDU consists of characters K28.2 and K27.7 which, assuming an initial negative disparity, will result in the following values after 8B10B conversion: 10'b0011110101 and 10'b0010010111 respectively. These two bit sequences would then be transmitted as: 0,0,1,1,1,1,0,1,0,1,0,0,1,0,0,1,0,1,1 and 1.

Figure 7 shows how a byte stream is output from an existing 8-bit Trace Port where Byte #0 represents the least significant byte of data. It is recommended that any STP implementation maintain this ordering of bytes within the data stream to ensure no mismatching of data which may occur due to internal port size constraints.

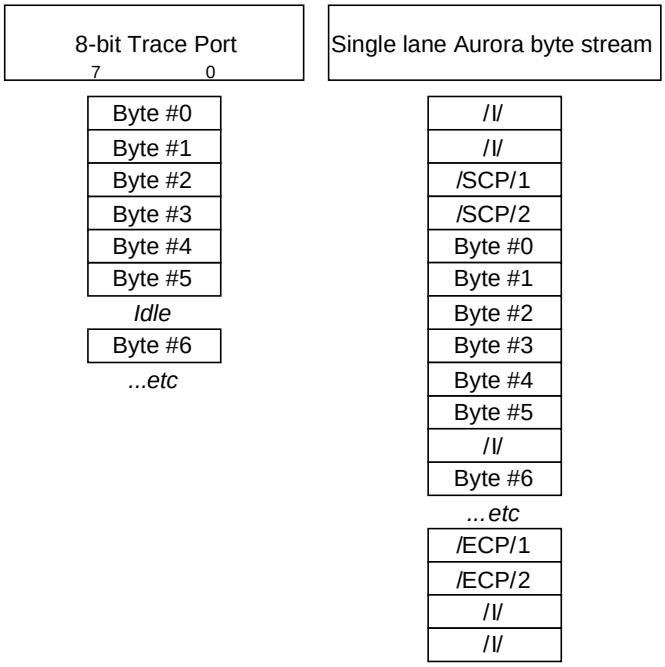


Figure 7: 8-bit parallel Trace Port byte ordering and Aurora byte ordering

The final data stream is output as a sequential stream of bytes, MSB first. Figure 8 illustrates the bit ordering within each byte of a 1-bit Trace Port against a pseudo-bit stream from Aurora (bytes are actually converted through 8B10B before being serialized). It also shows an alternative format (*Aurora protocol #alt*) that may be output by some HSSTP emitters.

Where an implementation outputs the trace data bit[0] first (LSB first, as shown by the Aurora protocol #alt in Figure 8), the LINK and PHY Capability register shall have the LINK_nDALT read LOW.

Where the HSSTP orders the trace data such that the MSB of each byte is output first (shown as the middle data stream in Figure 8), the LINK_nDALT should must HIGH.

More information about ordering of data is shown in Appendix C: Data byte ordering with example wiring connectivity to a Xilinx LogiCore.

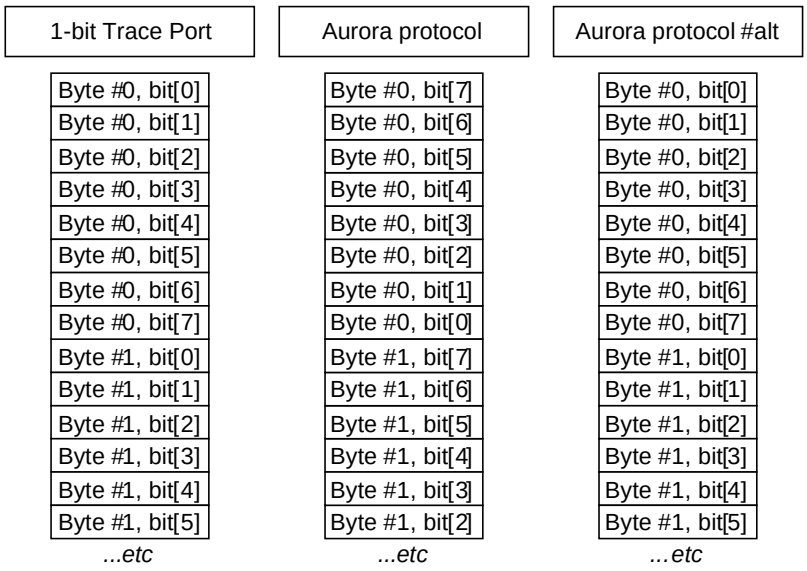


Figure 8: 1-bit Trace Port and Aurora bit stream ordering (without 8B10B encoding)

Note In Figure 8, the bit stream from Aurora is shown in two possible configurations for the orientation of the trace data before 8B10B encoding, however, for both implementations the framing octets must still be transmitted MSB first.

5.3 Error Conditions for DCD Rx Block

The quality of the STP to DCD transmission shall be such as to ensure error free transmission when the system is operating under normal conditions. An error indicator on the DCD (e.g. an LED lit or a message in the user interface) is intended to warn the user that error free transmission is not being achieved, that adverse conditions exist and need correcting.

The following sections describe the range of errors that can be detected. The DCD Rx block shall indicate to the user that any of the error condition has occurred. The DCD Rx block may indicate the error type.

5.3.1 Aurora generated error signals

HARD_ERROR

- The elastic buffer for Rx data overflows or underflows
- The protocol engine attempts to send a bad control character
- There are too many soft errors within a short period of time

SOFT_ERROR

- The 10-bit code received from the channel partner was not a valid code in the 8B/10B table
- The 10-bit code received from the channel partner did not have the correct disparity

FRAME_ERROR

- A frame is received with no data
- A frame is started without ending the previous frame
- A frame is ended without being started

- The protocol engine receives a control character that it does not recognize
- A UFC message is received with an invalid length
- An undefined UFC message is received

5.3.2 Error signals from outside Aurora

- Rx FIFO overflow
- Rx non-overflow FIFO error
- CRC error (qualified with CRC error valid signal)

5.4 Reset Requirements

The STP link reset requires that both transmit and receive sides be reset. The sequence of reset signal assertion on the Rx and Tx sides of the STP link is non-critical. The exiting of reset shall be ordered:

1. The DCD side reset is de-asserted.
2. The STP side reset is de-asserted.

This is a requirement to ensure that the receiver is ready to perform link initialization when the transmit side starts to perform this procedure. There is no requirement that both Rx and Tx sides are held in reset at the same time.

6 PROGRAMMER'S MODEL

The following registers shall be accessible by a debugger and in the SoC's memory map (IMPLEMENTATION DEFINED). All registers are 32 bits wide with unused locations ignored by tools and implemented as zero.

Note Any registers or bits required by the STP for diagnostic or debug purposes are not discussed below. These features are implementation dependent and must be placed as additional registers.

6.1 Summary

Table 3 gives an overview of the control and status registers specified within the HSSTP Architecture.

Table 3: STP Register Overview

R/W	Width	Name	Description
RO	9	STP Status Register	Indicates current operating state of the STP
R/W	5	STP Control Register	Primary control register, main enable register and reset controls
R/W	3	STP Lanes Select Register	Allows control over active lanes for transmission of trace data
R/W	16	PHY Clock Synchronization Register	Control register for adjusting the period between clock compensation sequences.
R/W	31	Link Initialization Register	Specifies the clock cycles used at the various stages of link initialization.
RO	14	LINK and PHY Capability Register	Indicates the current capability and operating mode of the STP.
RO	32	Link and PHY Identification Register	Identifies the designers of the link layer and PHY aspects within the STP.

6.2 STP Status Register

The STP Status Register allows the reporting of various conditions that the PHY and LINK layers may be in. This register is implemented as Read Only and any writes ignored. It is recommended that tools modifying any control registers should wait until the STP indicates that it is idle (CHANNEL_BUSY is LOW).

It is IMPLEMENTATION DEFINED if any disabled link lanes perform initialization and report HIGH for their status within LANE-UP. See Selected PHY Lanes Register and LINK and PHY Configuration Register for more information about enabled PHY and LINK lanes.

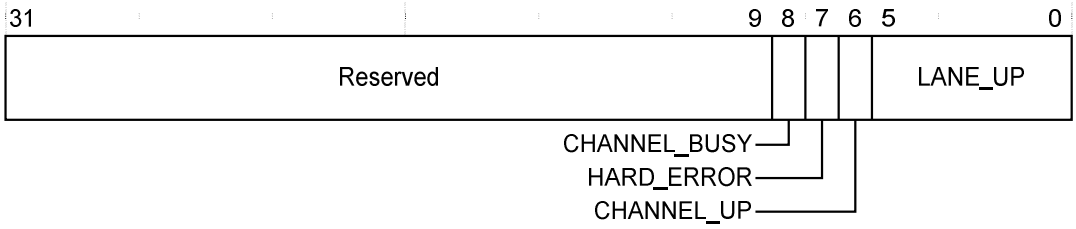


Figure 9: STP Status Register bit assignments

Table 4 shows the STP Status Register bit assignments.

Table 4: STP Status Register bit assignments

Bit	R/W	Name	Description
[31:9]		Reserved	RAZ/SBZP
[8]	RO	CHANNEL_BUSY	This will indicate HIGH when the STP is still processing data, this can be due to an existing Aurora frame being incomplete (not sent End-of-Frame packets), the LINK layer is being initialized or there is still data in buffers awaiting transmission.
[7]	RO	HARD_ERROR	Hard error on the channel. There is an error which requires a full reset of the link layer and PHY. See bit[2] of the STP Control Register. This might be the result of the elastic buffer for Tx data having an overflow or underflow.
[6]	RO	CHANNEL_UP	When HIGH, the channel is ready for data transmission.
[5:0]	RO	LANE_UP	Each bit represents the corresponding lane has been initialized. The lanes which can go HIGH is specified by the LINK_LANES configuration (see LINK and PHY Configuration Register) and the corresponding PHY enables within the Selected PHY Lanes Register.

6.3 STP Control Register

The STP Control Register allows for global enabling and disabling of the STP.

It is recommended that tools do not modify this register whilst the STP is active (see STP Status Register) and that when the STP is unused it should be left in the disabled state (STP_PWRUP is set LOW) when other control registers may be safely reprogrammed.

Disabling the STP while data is still being transmitted (or stored in any STP FIFOs) can result in the loss of trace data. To ensure all valid trace data is captured by the TPA, the STP should only be disabled following a flush of any trace FIFOs, including any FIFOs implemented within the STP.

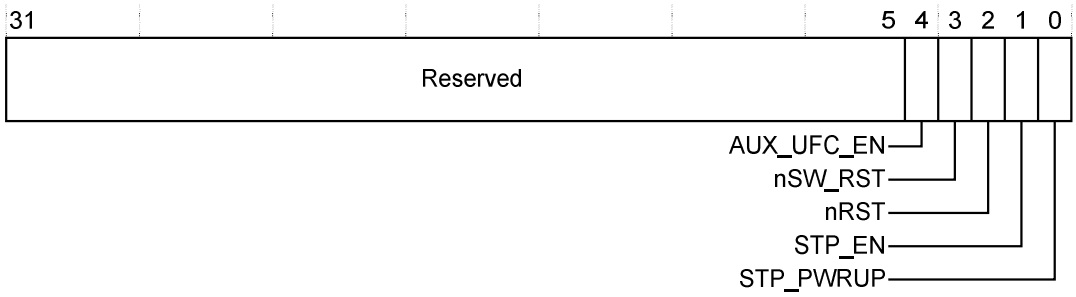


Figure 10: STP Control Register bit assignments

Table 5 explains the bit assignments for the STP Control Register.

Table 5: STP Control Register bit assignments

Bit	R/W	Name	Description
[31:5]		Reserved	RAZ/SBZP

[4]	RW	AUX_UFC_EN	This controls the output of the Auxiliary UFC packet within the Aurora data stream (see Auxiliary UFC Packet in 5.1.3 NFCs and UFCs for more information). The presence of this feature is IMPLEMENTATION DEFINED. Where not implemented this bit must always RAZ and ignore writes. This bit must reset LOW (disabled) where implemented for compatibility with tools that do not support receiving the Auxiliary UFC.
[3]	RW	nSW_RST	This is a soft reset of the link layer. No internal state change is lost however the link layer should cancel any transmit data which has not been sent. If the STP is in reset or disabled this bit should be held LOW. On completion of reset (or exit from system reset) this bit must go HIGH.
[2]	RW	nRST	This control is for a global STP reset. All internal state of the STP is reset to the power up default values. When the STP is in reset or disabled this bit should be held LOW. On completion of reset (or exit from system reset) this bit must go HIGH.
[1]	RW	STP_EN	STP data transmit enable. Setting this bit HIGH enables the transmission of trace data from the PHY. Reset LOW.
[0]	RW	STP_PWRUP	STP enable. Setting this bit HIGH enables the PHY and link layer ready for transmission. This should only be cleared when the STP is inactive as indicated by CHANNEL_BUSY (see STP Status Register). Reset LOW.

The usage of STP_EN and STP_PWRUP control bits are described in Table 6.

Table 6: Enable and power up control bits

Control bit	STP disabled	STP enabled, training patterns only	STP enabled, transmit data
STP_EN	X	0	1
STP_PWRUP	0	1	1

6.4 STP Lanes Select Register

This register allows control of the STP data output width and which lanes are active for a trace session. If an implementation does not allow different configurations then this register may be Read Only.

Where a Read Only value of zero is used in implementations, the value of LINK_LANES must indicate the correct number of lanes in use.

Tools should only perform writes of valid values to this register. Where an implementation supports multiple configurations, the valid values can be indicated in the LINK and PHY Capability Register.

Note For implementations which can support multiple configurations for the number of transmit lanes and have no bits set within bits [21:16] of the LINK and PHY Capability register then it is IMPLEMENTATION DEFINED as to the supported values that can be entered into the STP Lanes Select Register.

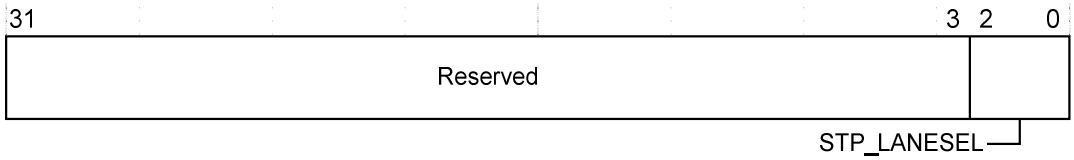


Figure 11: STP Lanes Select Register bit assignment

Table 7 gives the bit assignments of the STP Lanes Select Register.

Table 7: STP Lanes Select Register bit assignment

Bit	R/W	Name	Description
[31:3]		Reserved	RAZ/SBZP
[2:0]	RW	STP_LANESEL	This controls the number of active lanes used for transmitting the Aurora data stream. This value is one less than the actual number of lanes (a value of 0 corresponds to 1 lane selected). Values of 6 and 7 are reserved.

6.5 PHY Clock Synchronization Register

The PHY Clock Synchronization Register allows for the control of how regular the clock compensation packets are output. Implementations may implement this register as Read Only where it is not programmable (the clock compensation packets must not occur more than 10,000 symbols apart).

A read only value of zero will correspond to the compensation sequence being output every 10,000 symbols apart.

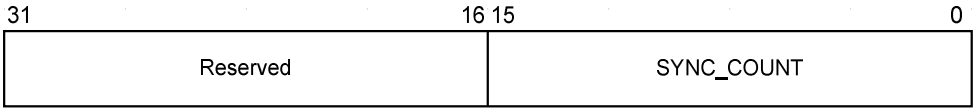


Figure 12: PHY Clock Synchronization Register bit assignments

Table 8 shows the bit assignments for the Clock Synchronization Register.

Table 8: Clock Synchronization Register bit assignments

Bit	R/W	Name	Description
[31:16]		Reserved	RAZ/SBZP
[15:0]	RW	SYNC_COUNT	The value in this register reflects the number of symbols transmitted between clock compensation sequences generated by the link layer. The reset value must be 0x2710 (decimal 10,000). Increasing the period between synchronization sequences is not recommended as corruption of trace can occur and may not be supported by the STP receiver fitted to the TPA. It is IMPLEMENTATION DEFINED how many of the SYNC_COUNT bits are writable, however where implementations restrict the write value, they must still allow the value of 0x2710 to be entered. Writing zero to this register is UNP.

6.6 Link Layer Initialization Register

The Link Layer Initialization Register controls the number of clock cycles used at the various stages of link initialization. The value of this register at reset is UNDEFINED and tools must initialize this register based upon the requirements of the receiver module.

This register must only be modified when the STP is disabled.

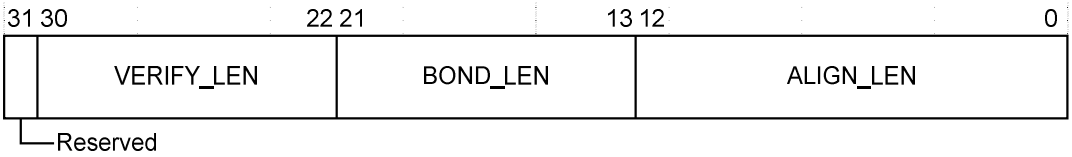


Figure 13: Link Layer Initialization Register bit assignments

Table 9 gives the bit assignments of the Link Layer Initialization Register.

Table 9: Link Layer Initialization Register bit assignments

Bit	R/W	Name	Description
[31]		Reserved	RAZ/SBZP
[30:22]	RW	VERIFY_LEN	The number of link layer clock cycles that the Aurora verification pattern must be sent by the Tx. Value = number of clock cycles - 1.
[21:13]	RW	BOND_LEN	The number of link layer clock cycles that the Aurora bonding pattern must be sent by the Tx. Value = number of clock cycles - 1.
[12:0]	RW	ALIGN_LEN	The number of link layer clock cycles that the Aurora alignment pattern must be sent by the Tx. Value = number of clock cycles - 1.

6.7 LINK and PHY Capability Register

This register indicates the current configuration and capability of the LINK and PHY implementation. For the majority of implementations of the HSSTP, this register is expected to be static; tools should check this register before programming to ensure the configuration has not been changed. The method of modification of the values displayed within this register is IMPLEMENTATION DEFINED and outside of the HSSTP Architecture.

Note Where an SoC supports multiple configurations, the LINK and PHY Capability Register shall reflect the current operational mode of the STP.

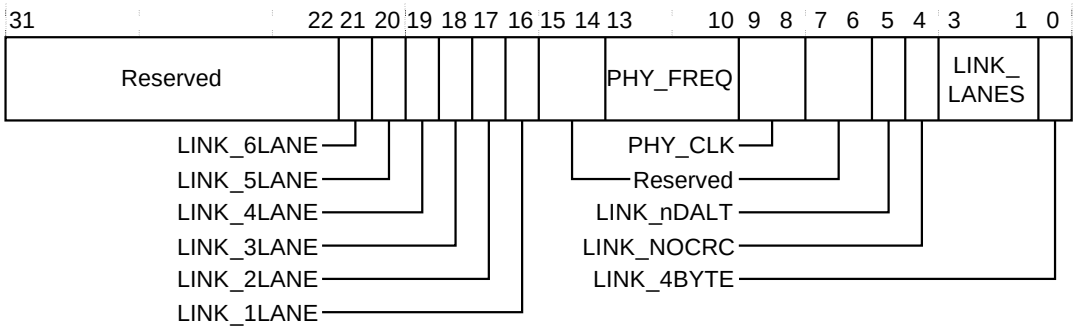


Figure 14: LINK and PHY Capability Register bit assignments

Table 10 gives the bit assignments of the LINK and PHY Capability Register.

Table 10: LINK and PHY Capability Register bit assignements

Bit	R/W	Name	Description
[31:22]		Reserved	RAZ/SBZP
[21]	RO	LINK_6LANE	Used to indicate that this implementation supports output of data over six lanes. Only valid when LINK_LANES is 6.
[20]	RO	LINK_5LANE	Used to indicate that this implementation supports output of data over five lanes. Only valid when LINK_LANES is 6.
[19]	RO	LINK_4LANE	Used to indicate that this implementation supports output of data over four lanes. Only valid when LINK_LANES is 6.
[18]	RO	LINK_3LANE	Used to indicate that this implementation supports output of data over three lanes. Only valid when LINK_LANES is 6.
[17]	RO	LINK_2LANE	Used to indicate that this implementation supports output of data over two lanes. Only valid when LINK_LANES is 6.
[16]	RO	LINK_1LANE	Used to indicate that this implementation supports output of data over a single lane. Only valid when LINK_LANES is 6.
[15:14]		Reserved	RAZ/SBZP
[13:10]	RO	PHY_FREQ	Indicates the clock frequency relationship in the PHY. See Table 11.
[9:8]	RO	PHY_CLK	Used to indicate the clock configuration used for the PHY. See Table 11.
[7:6]		Reserved	RAZ/SBZP
[5]	RO	LINK_nDALT	Indication as to the data byte ordering of the transmitted data. This should read HIGH when the data is sent in ordered sequential bytes, LSB first. See section 5.2 Trace data ordering for more information.
[4]	RO	LINK_NOCRC	Indicates the absence of a 2 byte CRC in the data frame. LOW when CRC is present, HIGH when CRC is absent.
[3:1]	RO	LINK_LANES	Indicates the number of lanes used for the transmission of trace data. This value is one less than the actual number of lanes (a value of 0 corresponds to 1 lane present). A value of 6 (3'b110) shall be used to indicate that the number of link lanes supported within this implementation is given within bits [21:16] (the LINK_xLANE indicator bits). A value 7 is reserved.
[0]	RO	LINK_4BYTE	Indicates the number of bytes per lane used in the link layer. LOW when only 2 bytes per lane are used; HIGH for 4 bytes.

Multiple bits within [21:16] may be HIGH to indicate that this implementation supports multiple configurations (selectable via the STP Lanes Select Register).

Table 11 describes the PHY configuration for the different clock and frequency options (PHY_CLK and PHY_FREQ respectively).

Table 11: PHY clock configurations

PHY_CLK[1:0] value	PHY_FREQ[3:0] values	Configuration
2'b00	4'b0000	Clock configuration A running at less than 2'5Gbps
	4'b0001	Clock configuration A running at 2.5 Gbps
	4'b0010	Clock configuration A running at 3.0 Gbps
	4'b0011	Clock configuration A running at 3.125 Gbps
	4'b0100	Clock configuration A running at 4.2 Gbps
	4'b0101	Clock configuration A running at 5.0 Gbps
	4'b0110	Clock configuration A running at 6.0 Gbps
	4'b0111	Clock configuration A running at 6.25Gbps
	4'b1000 to 4'b1111	Reserved
2'b01	4'b0000	Clock configuration B with the reference clock coming from the DCD through a 20x multiplier
	4'b0001	Clock configuration B with the reference clock coming from the DCD through a 25x multiplier
	4'b0010	Clock configuration B with the reference clock coming from the DCD through a 30x multiplier
	4'b0011 to 4'b1111	Reserved
2'b10	4'b0000	Clock configuration B with the reference clock not from the DCD
	4'b0001 to 4'b1111	Reserved
2'b11	4'b0000	Clock configuration C (2x multiplier)
	4'b0001 to 4'b1111	Reserved

6.8 LINK and PHY Identification Register

The LINK and PHY Identification Registers allows for the reporting where the LINK and PHY originated. Where the same manufacturer/designer was responsible for the link layer and the PHY then the LINK_ID and PHY_ID will be the same value.

The management of the version fields is the responsibility of the respective designers indicated within the ID field.

The STP Architecture must read as 0x0, indicating that it is following the architecture in this revision of the document.

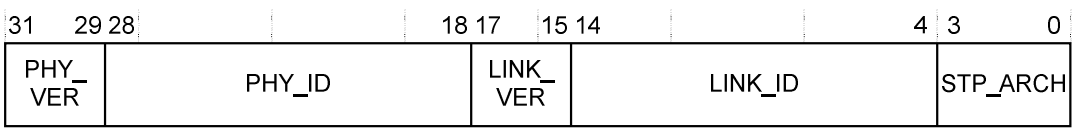


Figure 15: LINK and PHY Identification Register bit assignments

Table 12 shows the bit assignments for the LINK and PHY Identification Register.

Table 12: LINK and PHY Identification Register bit assignments

Bit	R/W	Name	Description
[31:29]	RO	PHY_VER	Revision of the PHY used
[28:18]	RO	PHY_ID	Short JEDEC code to identify the designer of the PHY used
[17:15]	RO	LINK_VER	Revision of the link layer design
[14:4]	RO	LINK_ID	Short JEDEC code to identify the designer of the Link Layer used
[3:0]	RO	STP_ARCH	STP architecture version. For this revision the field must read as 0x0.

7 CONNECTOR AND CABLE

In order to allow the design of Data Collection Devices (DCD) which are interoperable across multiple STP implementations, the connector and pin assignments specified below shall be used on all PCB assemblies.

The cable assembly used is considered part of the DCD designer's responsibility.

7.1 Connector

On target system PCBs, the connector used shall be the 40-way SAMTEC ERF8 with latching feature, part no. ASP-130367-01. The mating part on the cable/connector is the 40-way Samtec ERM8 with latching feature, part no. ASP-130365-01. This connector can support 10 Gbps and is therefore usable across multiple generations of STP drivers.

This part has 7 differential pairs and 20 single-ended signals assigned as shown in Table 13.

Table 13: Connector signal assignment

Signal	Pin	Pin	Signal
Tx4+	1	2	VTREF
Tx4-	3	4	TCK
GND	5	6	GND
Tx2+	7	8	TMS
Tx2-	9	10	nTRST
GND	11	12	GND
Tx0+	13	14	TDI
Tx0-	15	16	TDO
GND	17	18	GND
Clk+	19	20	nSRST
Clk-	21	22	DBGREQ
GND	23	24	GND
Tx1+	25	26	DBGACK
Tx1-	27	28	RTCK
GND	29	30	GND
Tx3+	31	32	TRIGIN
Tx3-	33	34	TRIGOUT
GND	35	36	Reserved
Tx5+	37	38	Reserved
Tx5-	39	40	Reserved
Ground	Latch	Latch	Ground

Note The connector is shown in its physical orientation. For example, Tx4+/Tx4- differential pair is located at the end of the connector. Pin assignment is shown in Figure 16.

Note Reserved are to be connected to ground, if not used.

In order to help the routing of the HSSTP differential pairs, the connector on the target PCB assembly should be orientated as shown by Figure 16. The diagram shows the view from above the PCB.

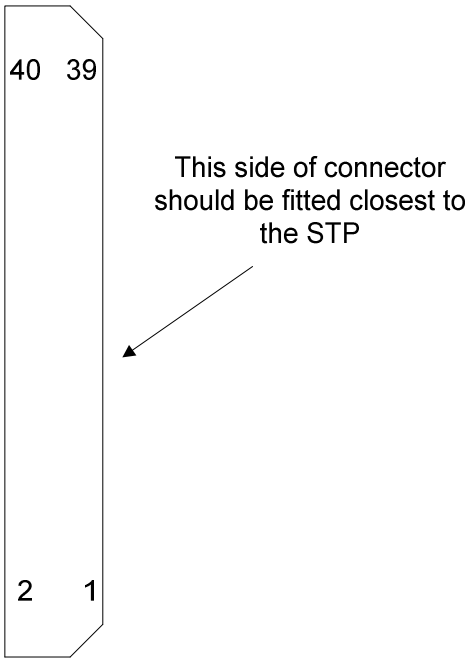


Figure 16: Connector pin assignment

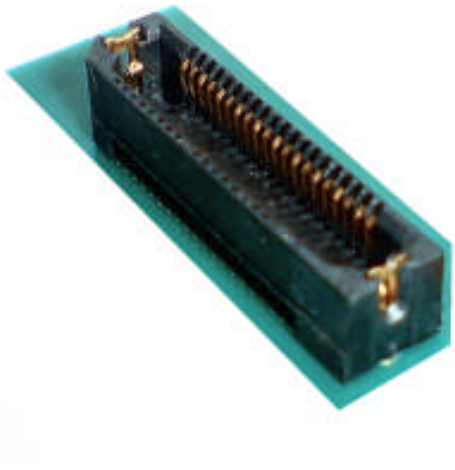


Figure 17: Samtec ERF8 connector with latches

Figure 18: Samtec ERM8 connector with latches

Note An edge-mounted version suitable for cable assembly is available (not shown).

7.2 Cable

The recommended cable for the STP is the Samtec Twinax 30AWG (low skew < 5ps) for differential pairs (odd pins) and Coax 38AWG for single-ended signals (even pins) or the Precision Interconnect “Blue Ribbon” series cable.

The frequency response for the Samtec Twinax 30AWG is provided in Appendix A.

8 APPENDIX A: CABLE FREQUENCY RESPONSE

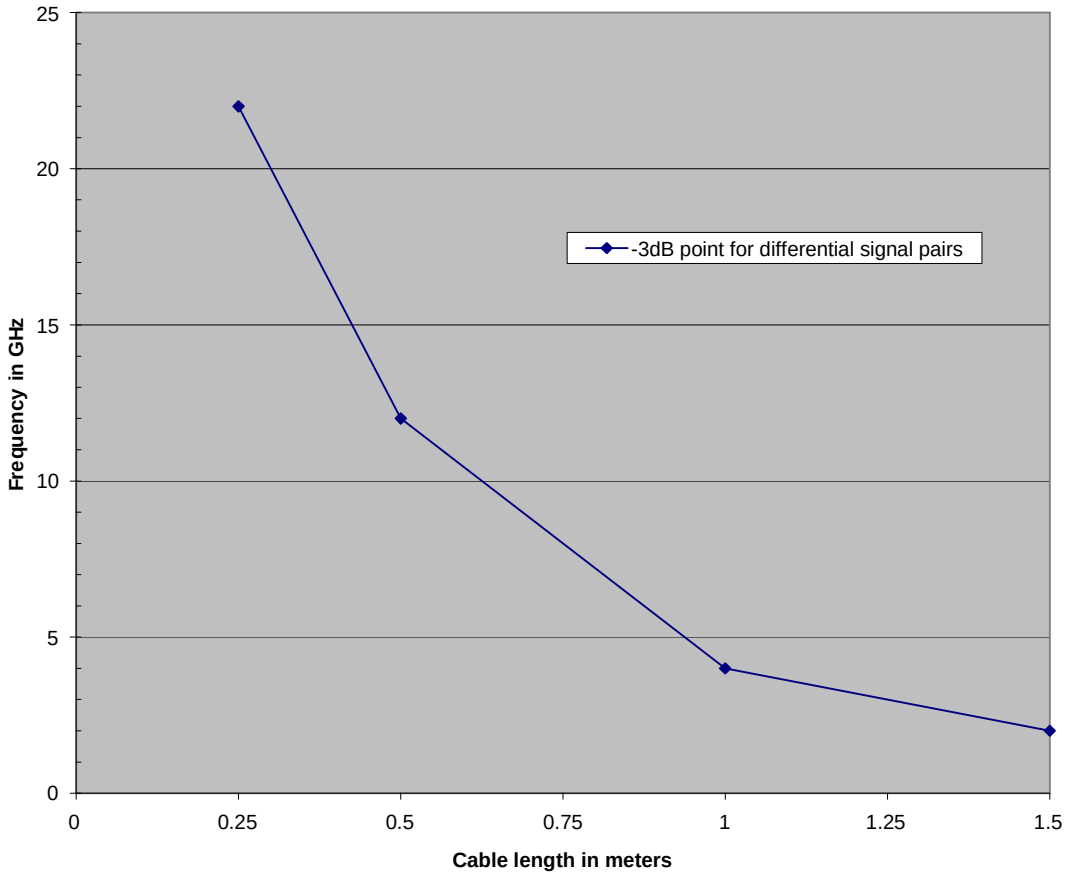


Figure A.1 Frequency response versus cable length for 30 AWG Twinax

9 APPENDIX B: ETM & CORESIGHT DATA REPRESENTATION

9.1 ETM to LINK Layer Connection

The Serial Transmit Port (STP) may be interfaced to both types of ARM defined Embedded Trace Macrocell (ETM) interfaces:

1. CoreSight ETMs with either of two interfaces:
   a. The CoreSight Trace Port Interface Unit (TPIU)
   b. The ETM Trace Port
2. Older ARM ETMs:
   a. ETM7 and ETM9 (ETMv1 architecture)
   b. ETM10RV and ETM11RV (ETMv3 architecture)

Note ETMs implementing ETMv2 protocols are not supported.

The signal mapping between the STP and ETM is described in table B.1 below.

STP	CoreSight or ETMv3	ETMv1
STP_TracePkt[0]	TraceData[0]	PipeStat[0]
STP_TracePkt[15:1]	TraceData[15:1]	TraceData[15:1]
STP_TracePkt[17:16]	TraceData[17:16]	PipeStat[2:1]
STP_TracePkt[18]	TraceData[18]	TraceSync
STP_TracePkt[19]	TraceData[19]	TraceData[0]
STP_TracePkt[31:20]	TraceData[31:20]	12'h000

Table B.1: STP to ETM and CoreSight signal mapping

9.2 Backwards Compatibility with Existing TPAs

An adapter may be designed to interface the STP to legacy Trace Port Analyzers (TPA) which collects parallel data from ETMv1.x and ETMv3.x protocols. This is implemented as specified below in table B.2.

Short name	Actual signal name	Trace Port Version
TD	TRACEDATA	ETMv3 & CoreSight TPIU
TC	TRACECTL	ETMv3 & CoreSight TPIU
PS	PIPESTAT	ETMv1
TS	TRACESYNC	ETMv1
TP	TRACEPKT	ETMv1

Table B.2: Table of abbreviated signal names

Most existing capture devices are designed to capture trace data from ETMv1 components which utilize a 4-bit pattern to indicate when valid data is present (i.e. something to store). With the introduction of ETMv3 and CoreSight, only 2 pins are used to indicate valid cycles, the other omitted pins require tie-offs to maintain compatibility with existing ETMv1 trace capture devices (see table B.3).

Note The STP does not transmit the TRACECTL pin and the TPA must re-create trace disable cycles when there is no data to emit.

ETM/CoreSight Protocol version	Required pattern for Trace Disable			
	Logic HIGH	Logic HIGH	Logic HIGH	Logic LOW
ETMv1	PS[0]	PS[1]	PS[2]	TP[0]
ETMv3 & CoreSight TPIU	TD[0]	TC	Tied HIGH	Tied LOW

Table B.3: Pin connections to indication non-capture cycles

9.2.1 Enhanced connection for ETMv1 and STP

The STP interface is designed primarily for CoreSight and ETMv3 trace. For existing ETMv1 devices, the TRACECTL input can be tied LOW which results in the transmission of data every cycle. An optimization to reduce the data transmission and only transmit cycles where data was present is shown in table B.4.

ETMv1 Signal(s)	STP Input Signal
(PS[0] & PS[1] & {PS[2] & ~TP[0])	TRACECTL
PS[0]	TRACEDATA[0]

Table B.4: Enhanced connectivity to correctly alter TRACECTL input of STP

9.2.2 STP output requirements for TPA compatibility

To ensure that existing TPAs do not need to be modified if an STP adaptor has been fitted, it must behave invisibly to the connected TPA. As the STP is primarily designed for ETMv3 or CoreSight trace sources, this is relatively simple with only the need to generate one signal (TRACECTL) and ensure that TRACEDATA[0] is HIGH.

For ETMv1 trace ports, all the data is sent over the STP channel to the output stage, however the location of the required signals are incorrectly located when the STP is connected to an appropriate ETMv1 TPA. To correctly interface to an ETMv1 TPA when using an ETMv1 trace port, a bit-shift is required to transfer transmitted information to pin-locations that are normally static or utilized for other purposes (see table B.3, noting that the STP interface is ETMv3/CoreSight in nature). To reduce the amount of pin multiplexing within the output stage of TPA Rx design, the input connections in table B.5 are recommended.

ETMv1 Signal	ETMv3 or CoreSight Signal	TPA Input pin
(PS[0] & PS[1] & PS[2] & ~TP[0])	TC	TC
PS[0]	TD[0]	TD[0]
TP[15:1]	TD[15:1]	TD[15:1]
PS[2:1]	TD[17:16]	TD[17:16]
TS	TD[18]	TD[18]
TP[0]	TD[19]	TD[19]
12'h000	TD[31:20]	TD[31:20]

Table B.5: Revised trace port and STP connections on the Tx side

ETMv1 input	ETMv3 or CoreSight input	Bit Pattern For Trace Disable cycles	ETMv1 based TPA Connections
Internal TD[0]	Internal TD[0]	1'b1	PS[0]
Internal TD[16]	Internally generated TC	1'b1	PS[1]
Internal TD[17]	Tied HIGH	1'b1	PS[2]
Internal TD[18]	Tied LOW	1'b0	TS
Internal TD[19]	Tied LOW	1'b0	TP[0]
Internal TD[15:1]	Internal TD[15:1]	15'bxxxxxxxxxxxxxxx	TP[15:1]
16'h0000	Internal TD[31:16]	TBD	Routed to 2nd TPA*

*ETMv1 trace components are restricted to a maximum 16-bit wide TracePkt.

Table B.6: Internal routing for STP output stage on the TPA Rx side

The following two diagrams represent tables B.5 and B.6.

Figure B.1 for an ETMv1 trace port connected to an ETMv1 designed TPA.

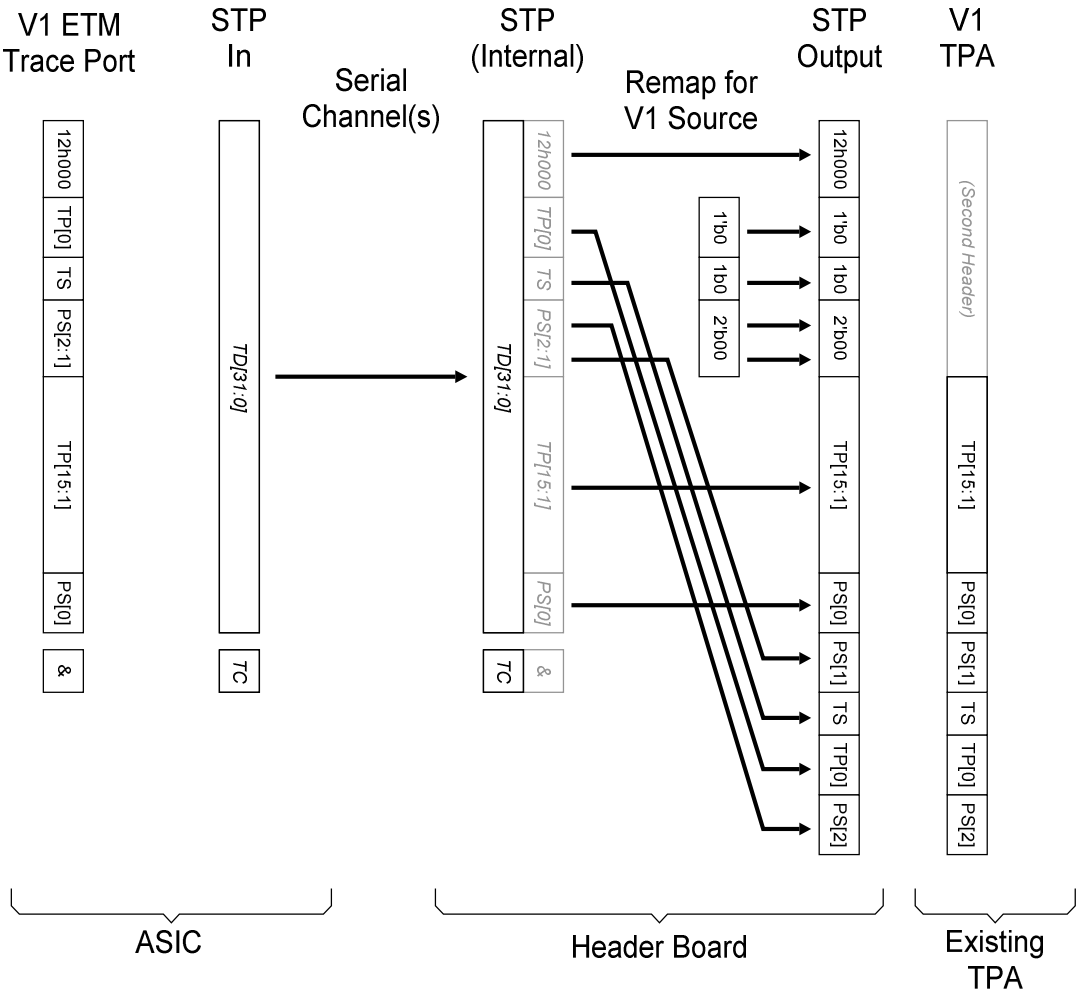


Figure B.1: STP connectivity for ETMv1 trace port and ETMv1 TPA

Figure B.2 shows an ETMv3 or CoreSight trace port connected to an ETMv1 designed TPA.

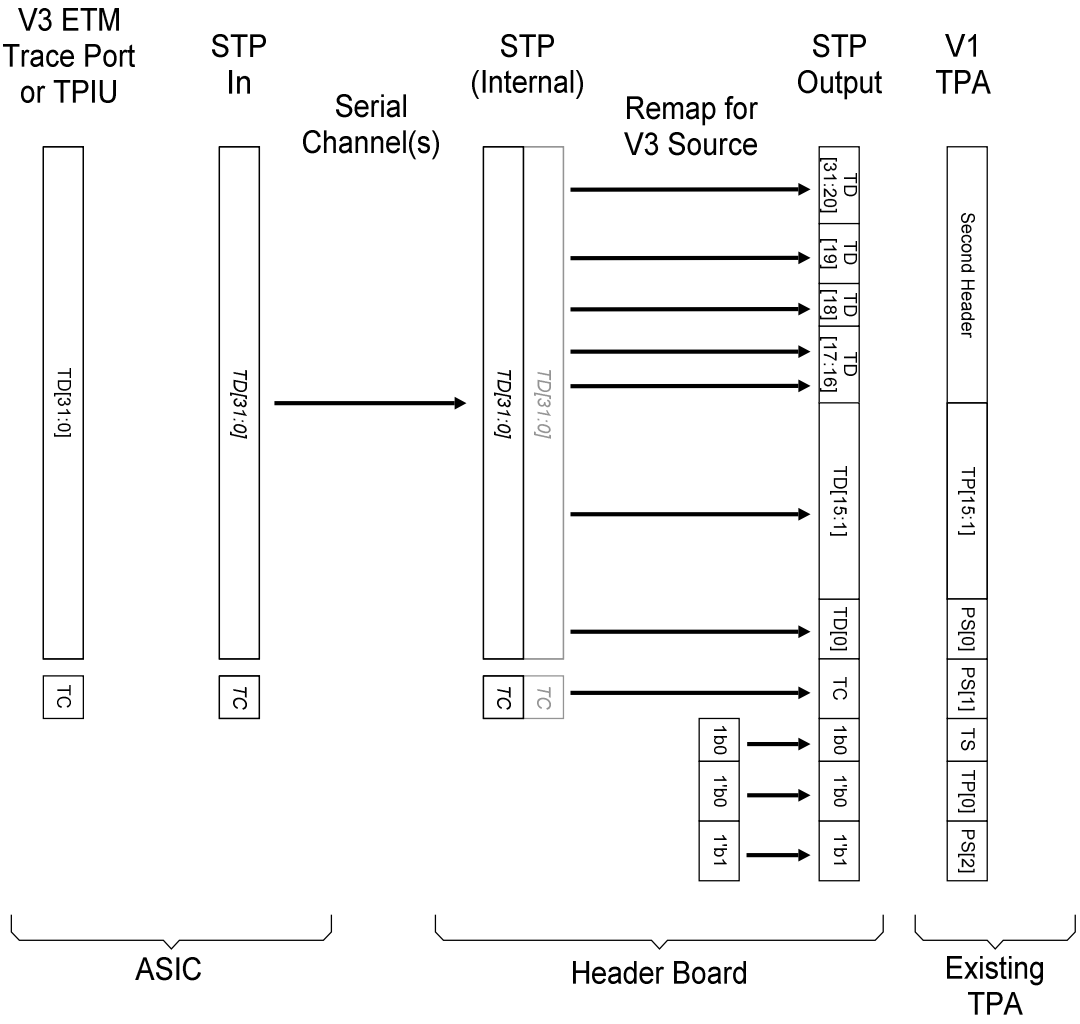


Figure B.2: STP connectivity for a ETMv3 or CoreSight trace port and ETMv1 TPA

10 APPENDIX C: DATA BYTE ORDERING

Within the CoreSight and ETM Architectures, the LSB (Least Significant Bit) is indicated as bit[0] of TRACEDATA and data transmitted should be treated as a bit stream, LSB first. Unfortunately within various Aurora documents bit [0] is used to indicate MSB first and sent most significant byte first.

10.1 Data ordering within CoreSight

Figure C1 shows the data ordering within the CoreSight Architecture which does not require the receiving unit to be aware of how long data sequences before data can be reconstructed.

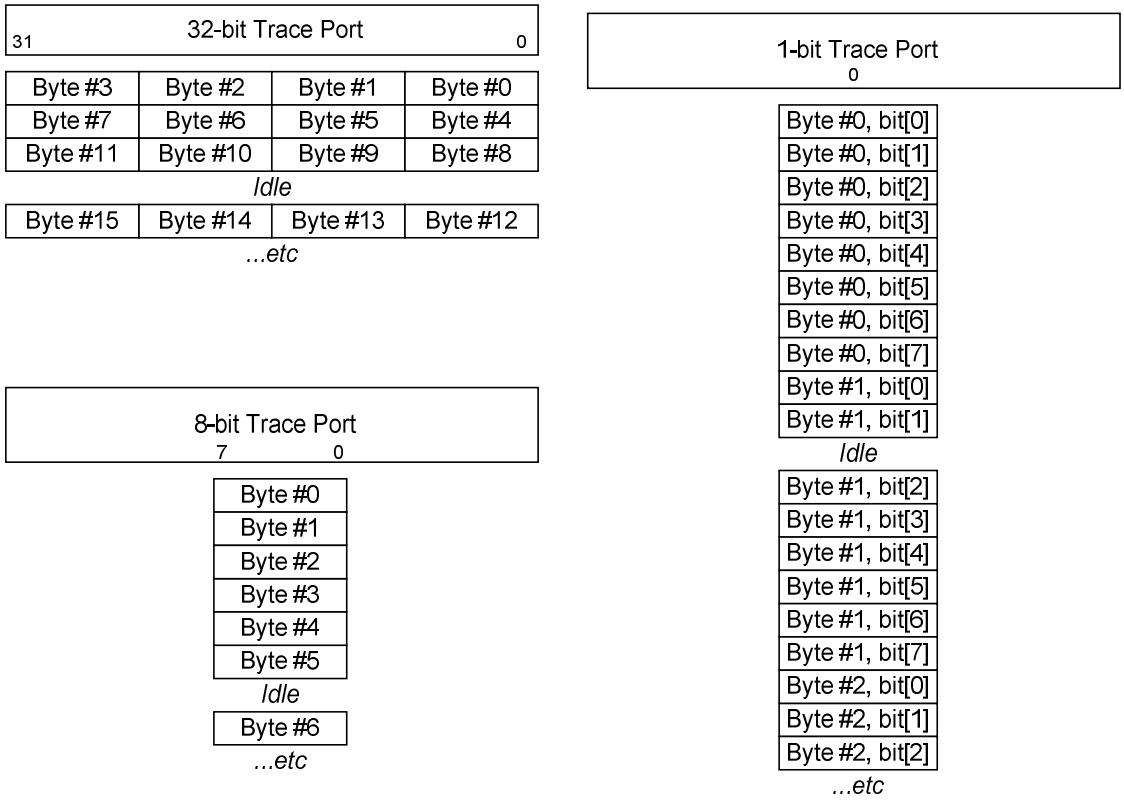


Figure C.1: Data ordering for different Trace Port data widths

10.2 Connecting a Trace Port to a Xilinx LogiCORE

Figure C.2 illustrates three different approaches to connecting a Xilinx LogiCORE (an implementation of the Aurora protocol). Due to the MSB/LSB identification used between the Trace Port and LogiCORE, the resultant data streams may result in an ordering different to what was desired.

Within Figure C.2, there are three example methods of connecting TRACEDATA[31:0] to TX_D[0:31]. In the first example they are directly connected (TRACEDATA[31] connected to TX_D[0]), the byte stream of data will be reverse ordered within word sequences. The resultant byte sequence, requires any receiving unit to be aware of the data width of this internal interface in order to correctly reorder the byte stream for arbitrary data streams.

Where TRACEDATA[0] is connected to TX_D[0] on the LogiCORE (the last example), the resultant data stream would have bytes transmitted LSB first. Implementations following this data ordering have the LINK_nDALT bit in the LINK and PHY Capability register read as LOW.

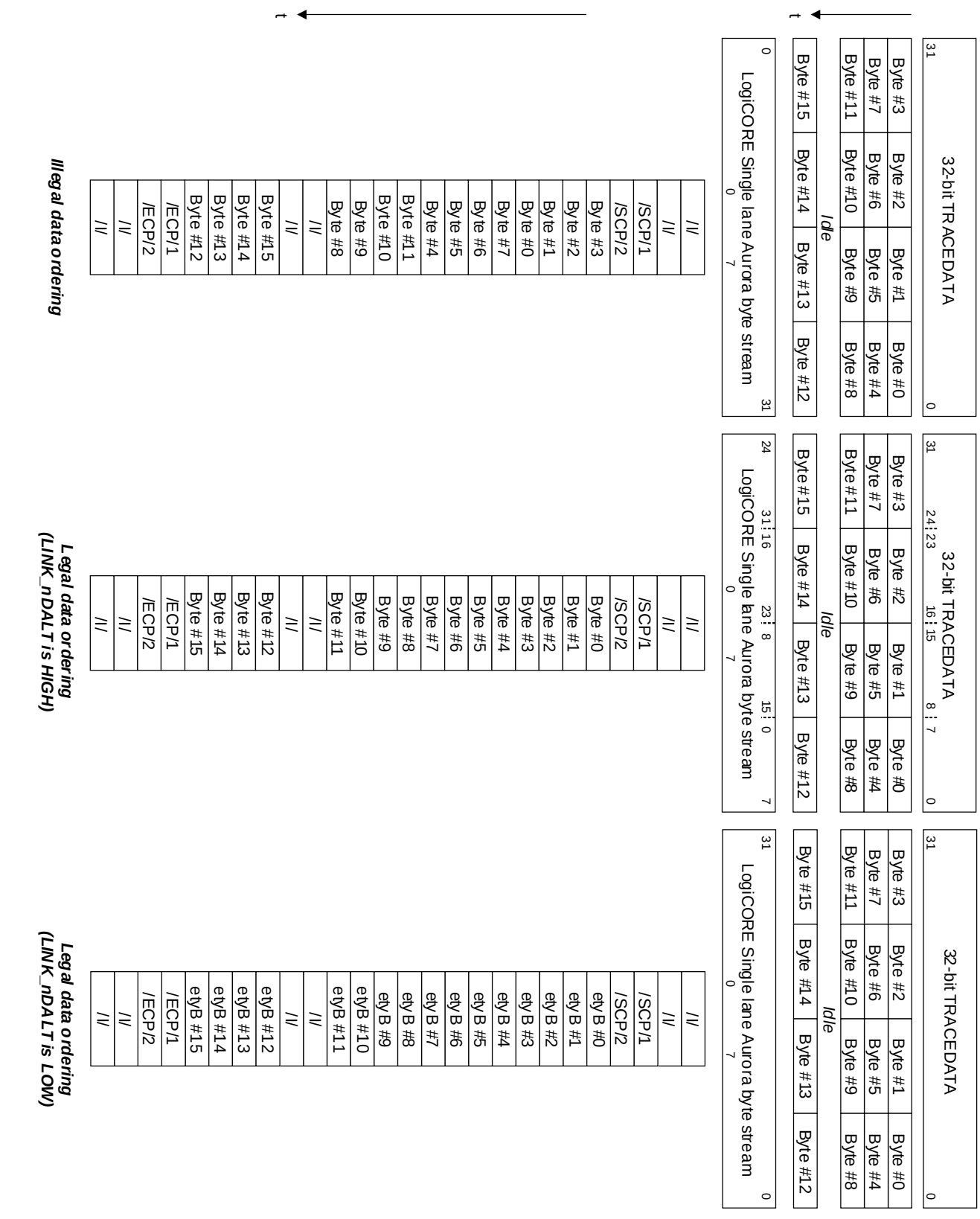


Figure C.2: Data ordering for different wiring schemes between a 32-bit Trace Port and a LogiCORE Aurora device